
# LightWise

## Line Scan Programmer's Manual

**FireWire™ / 1394a**
**Smart Digital Imaging Module**
**For**
**LW-ELIS-1024a-1394,**
**LW-SLIS-2048a-1394**
**&**
**LW-PE2K-CCD-1394**

**Line Scan Cameras**

**Register Details**

**Revision 2.5**


*Revision 2.5 Subject to change without notice.*

# Section 3: Programming Guide
## 3.1 Top Level Memory Map

| | | |
|---|---|---|
| Sensor Map | 0x000 - 0x3ff | B12 |

### Sensor Interface

| | | | |
|---|---|---|---|
| SICR | 0x400 | B15 | Sensor Interface Control (Control Register1) |
| SISTAT | 0x404 | | Sensor Interface Status |
| TRGDLY | 0x408 | U16 | Trigger Delay |
| STRBDLY | 0x40C | U16 | Strobe Delay |
| RTGDLY | 0x410 | U16 | Retrigger Delay |
| PWM | 0x414 | U8 | PWM Duty Cycle |
| STRADV | 0x418 | U8 | Strobe Advance |
| STRDUR | 0x41C | U16 | Strobe Duration |
| ILISCR | 0x424 | B10 | Linear Control Register (Control Reegister2) |
| SHUTTER | 0x428 | U16 | Shutter Value (LGINT on SLIS) |
| NUM_ROWS | 0x42C | U16 | Number of rows in a frame |
| VV_STRT | 0x430 | U12 | Start of line ROI |
| VV_END | 0x434 | U12 | End of line ROI |
| INT_COUNT_VAL | 0x43C | U11 | Short Integration for SLIS |
| NDRO_COUNT | 0x440 | U8 | NDRO Line count (ELIS Only) |
| DPR_DLY | 0x444 | U16 | DPR delay ELIS, Line Extend PE-2048 |
| CLKCR | 0x448 | U5 | Clock Divider/Control |
| PWM_SF | 0x44C | U8 | PWM Scale Factor (SLIS Only) |
| LRT_MULT | 0x450 | U9 | Line Rate Multiplier (SLIS Only) |

### Image Path Control

| | | | |
|---|---|---|---|
| IPCR | 0x800 | B14 | Image Path Control |
| IPSTAT | 0x804 | B2 | Image Path Status |
| HISTCOLSTRT | 0x808 | U12 | Histogram Window Column Start |
| HISTCOLWIDTH | 0x80C | U12 | Histogram Window Column Width |
| HISTROWSTRT | 0x810 | U11 | Histogram Window Row Start |
| HISTROWDEPTH | 0x814 | U11 | Histogram Window Row Depth |
| HISTCR | 0x818 | B4 | Histogram Control |
| HISTADDR | 0x81C | U5 | Histogram Address |
| HISTDATA | 0x820 | U26 | Histogram Data |
| DGAIN | 0x824 | U4.4 | Digital Gain |
| LUTADDR | 0x8B4 | U10 | Look Up Table Address |
| LUTDATA | 0x8B8 | U10 | Look Up Table Data |
| DOFF | 0x918 | U14 | Digital Offset |

## 3.2 Register Detail

**Note: Some data formats are given as (S/U # of integer bits. # of fractional bits). For example, S1.3 means the value can be either positive or negative with the first bit indicating the sign, one integer bit and three fractional bits. U0.8 means no sign bit (positive number), zero integer bits and eight fractional bits. Negative values must be programmed as 2's complement. A format of Bn means a binary format with n bits used.**

Address : 400x0 (SICR)
Data format : B15
Default Value: 00h

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Not used | TRIG_SEL | STRDUTR_ENA | LRTVMULT | Not used | | | SLIS_ENA |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Not used | TRGSNS | VIDEN | HTRIG | STRBM[1:0] | | TRIGM[1:0] | |

TRIGM: Trigger Mode. These bits control the trigger source as well as trigger operation for frame triggering.
TRIGM[1:0] = 00 : Local Trigger, One Shot
TRIGM[1:0] = 01 : Local Trigger, Retriggerable
TRIGM[1:0] = 10 : Host Trigger, One Shot
TRIGM[1:0] = 11 : Host Trigger, Retriggerable

**Local Trigger**: Trigger is input directly to camera via external connector.
**Host Trigger**: Trigger is issued via 1394 interface.
**One Shot**: Edge on trigger input initiates one video frame.
**Retriggerable**: Repeats Frames as long as trigger input is active. Time between frames controlled by **RTGDLY** register.

When in one-shot mode, integration time can be controlled by the FPGA, the IBIS sensor or the trigger duration. The control for this is located in Control Register 2. The table below shows some possible modes and register settings using an external trigger.

| Trigger Mode | TRIGM[1:0] | IBMODE[1:0] (Control Reg 2) |
|---|---|---|
| Trigger mode A (IIDC Trigger Mode 0) | 00b | 10b Use FPGA register to control integration time. |
| Trigger mode B (IIDC Trigger Mode 1) | 00b | 11b Use trigger duration to control integration time. |
| Trigger mode C | 01b | 01b Use sensor register to control integration time. |

STRBM : Strobe Mode. These bits control the functionality of the Strobe output to the illumination system.
STRBM[1:0] = 00 : Active high (Activated by trigger).
STRBM[1:0] = 01 : Active Low (Activated by trigger).
STRBM[1:0] = 10 : Always high (Not activated by trigger).
STRBM[1:0] = 11 : Always low (Not activated by trigger).

HTRIG : Host trigger bit. Asserted via 1394 interface.

VIDEN : Video Enable bit.

TRGSNS: Trigger Sense for frame trigger.

SLIS_ENA: This bit is set by the camera firmware. Do not change the value of this bit.

LRTVMULT: Line rate trigger video multiply enable (SLIS Only). When this bit is set and the camera is using the line rate trigger, the video output is scaled based on the incoming trigger. See section 2.2 for more information.

STRDUR_ENA: Strobe Duration Enable. This bit puts the strobe output in strobe duration mode. When in this mode, the strobe output has a duration of the vale set in register 0x41C.

TRIG_SEL: This bit selects what trigger input is used for frame rate triggering. When low, the differential input is used. When high, the opto-isolated input is used.

Address : 0x404 (TSTAT)
Data format : B1
Default Value: 00h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| not used | | | | | | | TSTAT |

TSTAT : Trigger Status. This read only bit is high when local trigger is asserted.

Address : 0x408 (TRGDLY)
Data format : U16
Default Value: 00h

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TRGDLY(15:8) | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TRGDLY(7:0) | | | | | | | |

TRGDLY : This 16 bit Value is used to program a delay from the time trigger is received to when strobe is activated. A delay between 0 and 1.37s in 20.83us steps can be achieved. The default value is 0.

Address : 0x40c (STBDLY)
Data format : U16
Default Value: 00h

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| Not Used | | | | | | STBDLY(17:16) | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| STBDLY(15:8) | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| STBDLY(7:0) | | | | | | | |

STBDLY : This 18 bit register is used to delay the strobe signal a programmed amount of time after the start of image acquisition. This delay is intended for use with flash illumination devices. This value can be programmed in steps of .65us to a maximum value of 170 ms. Note: The strobe delay must not exceed the image acquisition time. If a value is programmed for Strobe Advance the Strobe Delay value will be ignored.

Address : 0x410 (RTGDLY)
Data format : U16
Default Value: 00h

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RTGDLY(15:8) | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RTGDLY(7:0) | | | | | | | |

RTGDLY : This 16 bit Value is used to program the delay between video frames in continues trigger

Mode. A delay between 0 and 341ms in 5.21us steps can be achieved. The default value is 0.

Address : 0x414 (PWM)
Data format : U8
Default Value : 80h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PWM(7:0) | | | | | | | |

PWM : PWM Duty Cycle. This register controls the duty cycle of the 13Khz PWM signal fed to the illumination system. FFh = 100%, 80h = 50%, 00h = .4%.

Address : 0x418 (STRADV)
Data format : U8
Default Value : 0h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PWM(7:0) | | | | | | | |

STRADV : This 8 bit register is used to apply the strobe signal a programmed amount of time before the start of image acquisition to allow for illumination turn on time. This value can be programmed in steps of 5.21us to a maximum value of 1.33ms. Note: The trigger delay must be greater then the strobe advance.

Address : 0x41C (STRDUR)
Data format : U16
Default Value: 00h

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| STRDUR(15:8) | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| STRDUR (7:0) | | | | | | | |

STRDUR: This register is used to program the duration of the strobe pulse when strobe duration mode is enabled. This value can be programmed in steps of 5.2us to a maximum value of 341ms. Note: The strobe output will go inactive at the end of image acquisition no mater what the strobe duration is set to.

Address : 424x0 (LISCR)
Data format : B12
Default Value: 00h

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Not Used | | | | ELIS_LRT_MD[1:0] | | Not Used | PWM_SEL |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Not Used | INTC_MD | SLIS_MODE[1:0] | | ELIS_MODE[1:0] | | RUN_MODE | Not Used |

RUN_MODE: When low, the camera operates in continuous run mode. When high, the video is transferred on a frame-by-frame basis.

ELIS_MODE: Mode control for ELIS sensor.
00 = Dynamic Pixel Reset Mode
01 = Non Destructive Readout Mode
10 = Standard Mode

SLIS_MODE: Mode control for SLIS sensor.

INTC_MD: When set, the SLIS sensor runs in line trigger mode (SLIS only).

PWM_SEL: Selects between register controlled PWM output and line rate controlled PWM (SLIS only).

ELIS_LRT_MD:
ELIS line rate mode (ELIS only).
00 = Off
01 = Edge Mode
10 = Level Mode

Address : 0x428 (SHUTTER)
Data format : U16
Default Value : 0

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| SHUTTER/LGINT(15:8) | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SHUTTER/LGINT(7:0) | | | | | | | |

SHUTTER : Shutter value (ELIS + PE). The value in this register controls the integration time of the ELIS sensor when in Standard and NDRO modes. The electronic shutter is "open" (pixels accumulate light) for an amount of time as shown below.
Integration time = (Shutter Control Value + 1) * Clock Period.
For the PE camera, if the shutter value is greater than 2047, the line extend must also be increased to allow for the added integration time. For example, to set the integration time to 3048 clocks, the line extend must be set to a minimum of 1000.

LGINT : Long Integration Value(SLIS): When this register has a value of zero, the line rate is fixed at 2200T and the maximum integration time is 2047T. When this register is not zero, the maximum integration time and line time is extended by the value in this register.

Address : 0x42C (NUM_ROWS)
Data format : U16
Default Value: 512d

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| NUM_ROWS (15:8) | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NUM_ROWS (7:0) | | | | | | | |

NUM_ROWS: This register is used to program the number of rows in a frame.

Address : 0x430 (VV_STRT)
Data format : U12
Default Value: 0d

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Not Used | | | | VV_STRT (11:8) | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VV_STRT (7:0) | | | | | | | |

VV_STRT : Video Valid Start. This register along with the VV_END register determine what pixels that are to be used as valid video in the video output from the sensor. When this register is set to 0 and the VVEND register is set to 0x3FF, the line size of 1024 pixels is selected. The value in these registers does not affect any of the sensor timing.

Address : 0x434 (VV_END)
Data format : U12
Default Value: 2047d

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Not Used | | | | VV_END (11:8) | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VV_STRT (7:0) | | | | | | | |

VV_END : Video Valid End. See VV_STRT.

Address : 0x43C (INT_COUNT_VAL)
Data format : U11
Default Value: 7FFh

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Not Used | | | | INT_COUNT_VAL (11:8) | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| INT_COUNT_VAL (7:0) | | | | | | | |

INT_COUNT_VAL : Short Integration Control for SLIS. This register allows for integration times of less then one line. The value in this register determines the number of clock periods of integration for each line. The default (maximum integration) value is 2047d. The minimum is 5 clock period. The value in this register does not effect the line time of the sensor.

Address : 0x440 (NDRO_COUNT)
Data format : U8
Default Value: 0h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NDRO_COUNT (7:0) | | | | | | | |

NDRO_COUNT : Nondestructive Readout Line Count: This register determines how many times each line is re-read when in Non Destructive Read Out mode (ELIS Only).

Address : 0x444 (DPR_DLY ELIS, LINE_EXTEND PE)
Data format : U16
Default Value: 0h

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DPR_DLY/ LINE_EXTEND (15:8) | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DPR_DLY/ LINE_EXTEND (7:0) | | | | | | | |

DPRDLY (ELIS): Dynamic Pixel Reset Delay (ELIS Only): The value in this register is used to control integration time when in DPR mode. The minimum integration is controlled by the amount of time required to read the line of data out of the sensor. The value in this register will extend the integration time past this minimum time. For example:

Integration time = (Num of pixels read + DPR Delay Value + 2) * Clock Period.

The number of pixels read will depend on the resolution (binning control) setting of the sensor.

LINE_EXTEND (PE): The Line Extend value is used to extend the number of pixels in a line from 2200 (min when this register is zero) to 2200 + LINE_EXTEND reg value.
Line Time = (2200 + LINE_EXTEND) * Clock Period.

Address : 0x448 (CLKCR)
Data format : B12
Default Value: 02h

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Not Used | | | | CLK_STAT | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Not Used | | | OSCSEL | CLKDIV | | | |

CLKDIV: Clock Divide: The clock output to the sensor (pixel clock) will be divided by 2n. Where n is the value in this register.

OSCSEL: Oscillator Select: This register is used to select between a base frequency of 60 MHz or 48 MHz when set.

CLK_STAT: Clock DLL Status: These bits will be set when all of the FPGA DLLs are locked.

Address : 0x44C (PWM_SF)
Data format : U8
Default Value: 10h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PWM_SF (7:0) | | | | | | | |

PWM_SF : PWM Scale Factor: See section 2.2 for a description of line rate trigger and PWM scale factor. (SLIS Only).

Address : 0x450 (LRT_MULT)
Data format : U9
Default Value: 100h

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Not Used | | | | | | | LRT_MULT (8) |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LRT_MULT (7:0) | | | | | | | |

LRT_MULT: Line rate trigger multiplier: See section 2.2 for a description of line rate trigger. (SLIS Only).

Address : 0x824 (DGAIN)
Data format : U4.4
Default Value : 10h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DGAIN(7:0) | | | | | | | |

DGAIN : Digital Gain. The input video is multiplied by this value. The result is truncated to 1023. The range of DGAIN is 0 to 15.9375 in steps of 1/16. This value is R/W.

Address : 0x918 (DOFF)
Data format : S14
Default Value : 2000h

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Not Used | | DOFF[13:0] | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DOFF(7:0) | | | | | | | |

DOFF : Digital Offset. The input video is offset (+ or -) the value in this register. 0x2000 is zero offset.

# Calculating Integration Time and Line Time on the PE Lightwise Camera

The line time and integration time of the PE Lightwise camera can be independently controlled using two registers in the camera.

**The Integration Time Register 0x428** (also referred to as Shutter) controls how long the "electronic shutter" is open for a given line. The register has a range of 0 – 65535 in units of clock periods (T=1/36 MHz). For the maximum line rate, the integration register is limited to 2047T. To increase the integration time beyond 2047T the line time needs to be extended.

**The Line Extend Register 0x444** controls how many clock cycles are added to the default minimum number of clock cycles in a line. The default minimum is 2200T. The sensor requires an overhead of 152T (152T + 2048T = 2200T). Increasing the value in this register will slow the sensor line rate down. This register also has a range of 0 – 65535 in units of clock periods (T=1/36 MHz). It is possible to extended the line time without increasing the integration time.

Equations: **Line time = (2200 + Line Extend Register) * T** **Integration time = Integration Register * T**
**Note: The line time must always be at least 152T larger than the sensor integration period.**
So if the integration Register has a value larger than 2047, the minimum value in the line extend register = Integration Register - 2047

Example #1:
Minimum line time with integration time of 10uS
Minimum Line time is required so set the Line Extend Register = 0
Integration Register = 10 us*36 MHz = 360 (0x168)

Example #2:
The smallest line time possible with an integration time of 1mS
Integration Register = 1mS*36 MHz = 36000 (0x8CA0)
In order to accommodate this integration, the line time must be extended by an amount = 36000 - 2047 = 33953 (0x849F)

Example #3:
Line time = 2 mS and an integration time = 1 mS
Integration Register = 1mS*36 MHz = 36000 (0x8CA0)
Line Extend Register = 2mS * 36 MHz – 2200 = 69800 (110A8)